20V Wireless Charging Transmitter Full-bridge Power Chip CH275

Datasheet

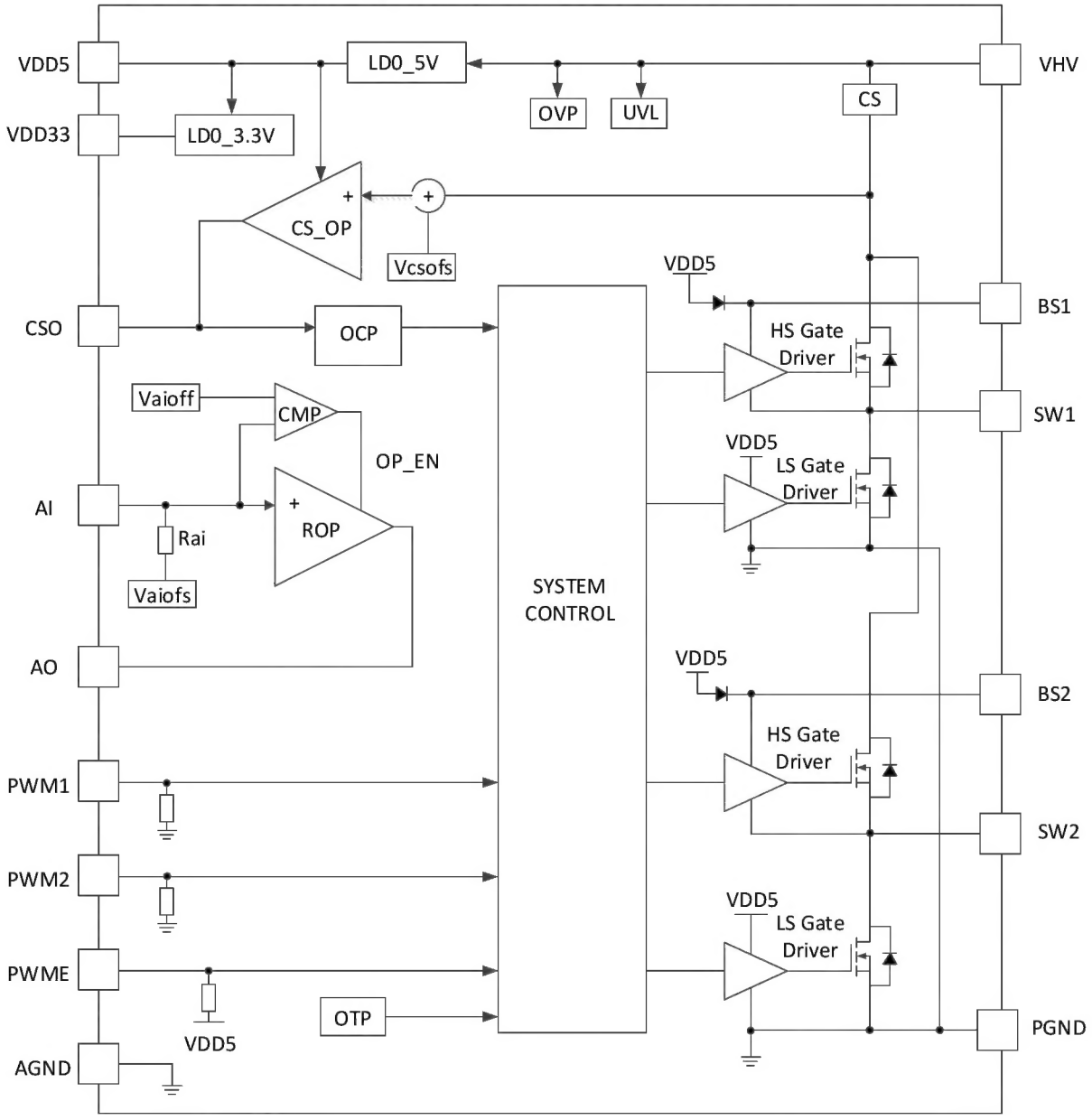
Version: 1.3

https://wch-ic.com

1. Overview

CH275 is a full-bridge power chip with four built-in power switching tubes and current sampling module and wireless charging feedback signal amplifier module. The chip integrates over-current protection, over-temperature protection, over-voltage protection, under-voltage lockout and other modules, supports FOD foreign object detection, and has a built-in LDO regulator to provide 5V or 3.3V power supply for the MCU, with streamlined peripheral devices, which can be used for the transmitter side of the wireless charging or motor drive.

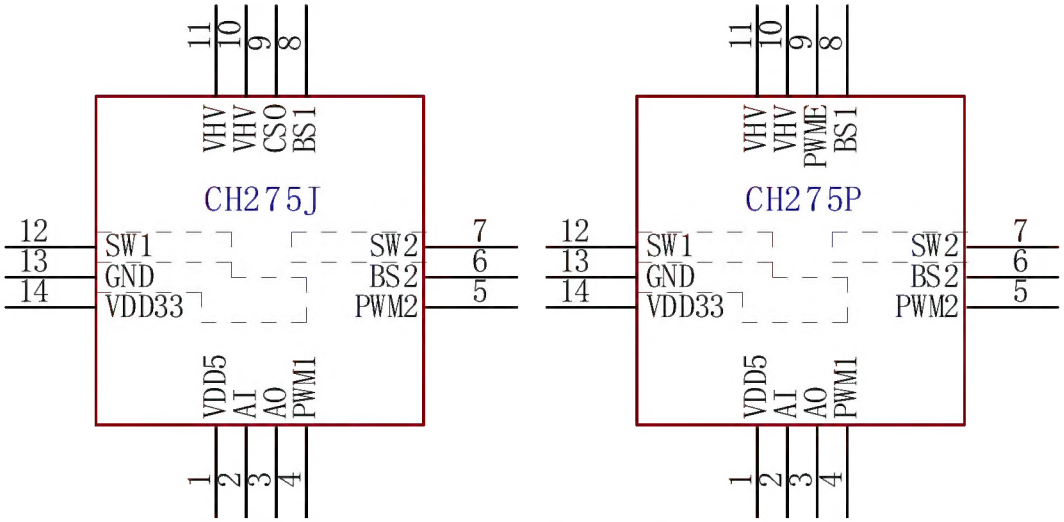
The following is the internal block diagram of CH275 for reference only.



2. Feature

- Built-in 4 N-MOSFET power switching tubes, typical 20mΩ on-resistance.
- Rated 2A continuous on-state current, supports 5A peak current.
- Built-in low dropout bootstrap diode, peripheral only need capacitor.
- Built-in Current-Sense current sampling and amplification circuit, supports FOD foreign object detection.
- Built-in wireless charging feedback signal amplifier module ROP, supports MCU signal demodulation.
- Built-in power tube over-current protection module OCP.
- Built-in chip over-temperature protection module OTP.
- Built-in power supply over-voltage protection module OVP and power supply under-voltage lockout module UVL.
- Built-in LDO low dropout regulator, generates 5V and 3.3V for MCU simple power supply.
- PWM input control signal level compatible with 5V, 3.3V and 2.5V voltage MCU or FPGA.
- Integrated dead-time control, supports PWM up to 500KHz switching frequency.
- Support 5V, 9V, 12V, 15V, 20V and other power supply voltages, high energy conversion efficiency.
- Available in QFN14F and other packages.

3. Pinouts



Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN14F	3*3mm	0.5mm	19.7mil	Quad Flat No-lead Package	CH275J
QFN14F	3*3mm	0.5mm	19.7mil	Quad Flat No-lead Package	CH275P

Note: Pin 0# refers to the EPAD of the QFN package, and pin 0# has been connected to pin 13# as a single unit. Reservation is required for CH275P.

4. Pin Definitions

Pin No.		Pin name	Type	Pin description
275J	275P			
12	12	SW1	Output	Output of half bridge 1, switch node 1, is in phase with PWM1.
7	7	SW2	Output	Output of half bridge 2, switch node 2, is in phase with PWM2.
8	8	BS1	Power	The VBS supply for the gate drive of the high-side power tube of half-bridge 1 is bootstrapped by connecting SW1 through a 0.1uF capacitor
6	6	BS2	Power	The VBS supply for the gate drive of the high-side power tube of half-bridge 2 is bootstrapped by connecting SW2 through a 0.1uF capacitor
4	4	PWM1	Input	Input of half bridge 1, PWM control signal, built-in weak pull-down resistor.
5	5	PWM2	Input	Input of half bridge 2, PWM control signal, built-in weak pull-down resistor.
10,11	10,11	VHV	Power	Power supply input, positive voltage terminal of the full bridge, with at least two 10uF high-frequency capacitors connected externally immediately to the pins
1	1	VDD5	Power	Internal 5V voltage regulator LDO output, close to the pin and externally connected with at least 1uF capacitor, 2.2uF or more is recommended.
Internal	Internal	PGND	Power	Ground terminal of power supply, negative voltage terminal of full-bridge
Internal	Internal	AGND	Power	Common ground terminal, negative voltage terminal of the whole system.
13,0	13,0	GND	Power	Common ground, equivalent to internal PGND and AGND short circuit.
9	None	CSO	Output	Current sampling is converted into voltage amplification and then output.
2	2	AI	Input	The input of the signal amplification module has been provided with DC bias internally, and the external input must be isolated from DC. Short AI to VDD5 to close this module.
3	3	AO	Output	Output of amplification module ROP of wireless charging feedback signal
14	14	VDD33	Power	Internal 3.3V LDO output, external capacitor when used.
None	9	PWME	Input	PWM global enable control signal with built-in weak pull-up resistor.

5. Function module

5.1 Full-bridge Switch and Its Drive

The full-bridge switch consists of a half-bridge 1 and a half-bridge 2. Each half-bridge consists of 2 N-type MOSFET, a low-side power transistor and a high-side power transistor, their respective gate driving modules, and a dead-time control module. VDD5 provides power for the low-side power transistor and its gate drive; The BS1/BS2 pin provides power for the high-side power tube and its gate drive. The bootstrap high voltage is obtained by the built-in ultra-low voltage drop ideal diode and a passive energy storage capacitor at the periphery to realize VBS power supply. The capacitor supports the range of 10nF ~ 1uF, usually 0.1uF is selected.

The input control signal of half-bridge 1 is PWM1, and the output is SW1, which is in phase with PWM1 and completely controlled by PWM1. After the input of PWM1 becomes low level, the high-side power tube is turned off first, and then the low-side power tube is turned on later, and SW1 is short-circuited to PGND; After the PWM1 input becomes high, the low-side power tube is turned off first, and then the high-side power tube is turned on later, and SW1 is short-circuited to VHV. The above-mentioned first turning off and then turning on later is realized by the internal dead-time control module, which is used to avoid the damage caused by the large current caused by the simultaneous conduction of the high and low power tubes. PWM1 signal usually comes from MCU or FPGA, which supports 5V or 3.3V and 2.5V signals.

Half-bridge 2 is similar to half-bridge 1, and SW2 is controlled by PWM2. The two half-bridges are independent of each other, and the combination of PWM1 and PWM2 can drive SW1 and SW2 to realize 4 output combinations.

PWME is the PWM global enable control signal. PWME high level enables PWM and turns on CS current sampling and amplification. PWME low level disables PWM and CS circuits to reduce power consumption, and turns off SW1 and SW2 and sets the output to 3 states. PWME does not affect ROP.

There is a parasitic diode in the power tube with the opposite polarity to the current when it is turned on normally, which can be used to maintain free-wheeling for the inductive load when the power tube is turned off. However, the diode has a large voltage drop, so it is suggested to avoid overheating caused by long-term free-wheeling and high-power driving when it is empty.

5.2 Power System

The VHV supplies full-bridge power and LDO regulators and supports supply voltages rated at 5V, 9V, 12V, 15V and 20V. VHV also supports supply voltages in excess of 21V for applications with PWM frequencies below 200KHz, good heat dissipation and low reliability requirements.

When working, the ripple of VHV is large, so it is necessary to place 2 low ESR high-frequency capacitors not less than 10uF close to VHV and GND pins. For example, two 22uF MLCC capacitors are connected in parallel.

VDD5 generates 5V power supply from VHV by built-in LDO, and it needs to place low ESR high-frequency capacitors in the range of 1uF~4.7uF close to VDD5 and GND pins, which can be used to supply power to the gate drive module, bootstrap power supply, dead-time control module, current acquisition and operational amplifier of low-side power tube, and can also be used to provide simple 5V power supply of less than 20mA for MCU. Note that when VHV is only 5V, the output of VDD5 will be less than 5V.

VDD33 generates a 3.3V regulated power supply from VDD5 by the built-in LDO, which can be used to provide a simple 3.3V power supply of no more than 20mA for the MCU, with external high-frequency capacitors in the range of 0.1uF to 4.7uF as needed, and no external capacitors are required when not supplying power to peripherals such as the MCU.

5.3 Current Sampling CS and Amplification

CH275 has built-in Current-Sense current sampling, which is converted into voltage and amplified, and then output from CSO pin. Because of the noise of switching pulse, it is suggested that CSO voltage signal be filtered by RC low-pass before being connected to ADC pin or comparator of MCU. To remove the effects of chip misalignment and dispersion, this voltage is superimposed on the DC bias voltage Vcsofs, which is more discrete, and the MCU needs to calculate the current by subtracting the ADC value when there is current from the ADC value when there is no current, and dividing the current by the coefficient Gcs in terms of the voltage difference corresponding to the ADC difference. The built-in current sampling is discrete and nonlinear, and the internal resistance of GND package or PCB wiring resistance will also affect Gcs. Therefore, the current value is mainly used for rough control and relative comparison, such as current signal demodulation or FOD foreign body detection, and is not suitable for precise calculation.

Reference calculation formula: Ifb = (Vcso – Vcsz)/Gcs

For example, Gcs=0.58, the CSO voltage Vcsz when PWM is off and there is no current is 0.8V, and the CSO voltage Vcso when there is current after switching on is 1.09V, then the full-bridge current Ifb = (1.09-0.8)/0.58 = 0.5A; If Vcso is 2.54V, Ifb=(2.54-0.8)/0.58=3A.

Considering that the internal resistance or PCB alignment of half-bridge 1 and half-bridge 2 may not be the same, it is recommended to use the average current sample value, which is RC low-pass filtered and contains multiple PWM cycles, as the result.

5.4 Amplification of Feedback Signal at the Receiving End

CH275 has a built-in amplifier module ROP for wireless charging feedback signal, with AI pin as input and AO pin as output. Chip internal AI pin has been provided for the DC bias voltage Vaiofs, external diode detector out of the wireless charging feedback signal should be low-pass filtering, and then through the capacitor isolation of DC portion of the input, in the chip after the internal amplification of the Gop times, the output from the AO pin, it is recommended that the RC low-pass filtering, capacitance isolation of the AC coupling to the MCU's signal capture inputs or interrupt the input pin signal demodulation, the MCU pin can be referenced to the pin input flip flop voltage with two resistor divider. MCU pins can be referenced to the pin input flip-flop voltage is divided with two resistors to provide DC bias.

If the AI pin is short-circuited to VDD5 and meets the turn-off voltage Vaioff, the amplifier module can be turned off to reduce the static current.

5.5 Overvoltage Protection OVP

CH275 has built-in overvoltage protection module, which continuously monitors the VHV voltage. When the VHV power supply voltage is too high, it will forcibly close the full-bridge switch.

5.6 Undervoltage Locking UVL

CH275 has built-in undervoltage locking module, which continuously monitors VHV voltage and VDD5 voltage. When VHV power supply voltage is too low or VDD5 voltage is too low, the full-bridge switch will be forced to close.

5.7 Overcurrent Protection OCP

CH275 has built-in overcurrent protection module, which continuously monitors the results of current sampling. When the current is too large and lasts for several microseconds, overcurrent protection will be triggered. After triggering OCP/OVP/UVL protection, the full-bridge switch will be closed briefly, and after waiting for several PWM cycles, it will be allowed to work again.

5.8 Overtemperature Protection OTP

The power consumption of CH275 mainly includes: power switch tube turn-on voltage drop multiplied by current, parasitic diode freewheeling voltage drop multiplied by current, LDO voltage drop multiplied by its own and MCU load current. Excessive power consumption as mentioned above or other abnormal power consumption may cause the chip to heat up internally. the CH275 has a built-in temperature detection module, which triggers the over-temperature protection when it detects that the chip temperature has reached the over-temperature protection point Tsd, turning off the full-bridge switch until the chip temperature is lower than the low-temperature hysteresis point Ton of the over-temperature protection, and then it will be allowed to work again. If it over-temperatures for a period of time after it is turned on, it will be turned off again.

6. Parameters

6.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter description		Min.	Max.	Unit
TA	Ambient operating temperature	VHV<21V	-40	85	℃
		VHV>=21V	-20	70	℃
TJ	Operating junction temperature		-40	150	℃
TS	Ambient temperature during storage		-55	150	℃
VHV	Power supply voltage of VHV pin		-0.4	27	V
VSW	Tolerant voltage of SW1/SW2 pin		-0.4	VHV+0.4	V
VBS	Power supply voltage driven by the gate of the BS1/BS2 pin.		-0.4	VSW+6	V
VPWM	Signal voltage of PWM1/PWM2/PWME pin.		-0.4	7	V
VIO	Signal voltage of other pins such as AI/AO/CSO.		-0.4	VDD5+0.4	V
VESD	HBM mannequin ESD tolerant voltage		2		KV
IAVQ	Continuous conduction current of QFN14F package			3.5	A
PD	Maximum power consumption of chip (including power tube and LDO power consumption)	QFN14F		600	mW
θ_{JA}	Packaging thermal resistance	QFN14F	90		℃/W

6.2 Electrical Parameters (Test conditions: TA=25℃, VHV=5V~20V)

Name	Parameter description		Min.	Typ.	Max.	Unit
VHV	Power supply voltage of VHV pin		4	5～20	22	V
VDD5	Supply voltage of LDO output at VDD5 pin.	4.9	5.0	5.1	5.15	V
		4.6	4.8	5.0	5.0	V
VDD33	Power supply voltage of VDD33 pin LDO output		3.2	3.3	3.4	V
Ildo	VDD5 and VDD33 add up the output load current.				20	mA
Vovp	Voltage threshold of OVP overvoltage protection		24.5	25.5	26.7	V
Vuvl	Voltage threshold of UVL undervoltage locking	3.3	3.5	3.8	3.8	V
		2.3	2.5	2.9	3.0	V
Iq0	PWME=GND and AI=VDD5, Static current after turning off ROP and CS			70	120	uA
Iq	Static current after closing ROP with PWME floating and AI=VDD5			500	800	uA
Iqop	Static working current after ROP is turned on (default state)			820	1200	uA
Vil	Low input voltage of PWM1/PWM2/PWME pin.		0		0.8	V

Vih	High input voltage of PWM1/PWM2/PWME pin.		2.2		5	V
Ipu	Pull-up current of PWME pin	2	4	7	7	uA
		60	100	150	150	uA
Ipd	Pull-down current of PWM1/PWM2 pin.		4	10	18	uA
Fpwm	Signal frequency of PWM1/PWM2 pin.		10		500	KHz
Ron	On-resistance of single power tube of full-bridge switch		20	30	30	mΩ
Tsd	OTP over-temperature protection threshold (with hysteresis)	120	135	150	150	°C
Ton		70	95	115	115	°C
Iocp	Current threshold of OCP overcurrent protection	5	7	15	15	A
Vcsofs	DC bias voltage of CSO current sampling results		0.01	0.8	1.6	V
Gcs	Ratio of CSO output voltage difference to sampling current difference	0.45	0.58	0.7	0.7	V/A
Rcs	Load resistance range of CSO output		12			KΩ
Vaiofs	DC bias voltage at ROP input AI		1.2	1.5	1.8	V
Vaioff	AI input voltage required to turn off ROP		VDD5-0.7	VDD5	VDD5	V
Rai	Input impedance (bias resistance) of ROP input AI		70	100	130	KΩ
Gop	Magnification of ROP signal amplification module		20	21	22	mV/mV
Rop	Load resistance range of AO output		10			KΩ

7. Application

CH275 has a larger average working current and a larger peak current. It is suggested to use more vias and wider line width in PCB design, pay attention to the current direction and consider the heat dissipation of the chip, especially the connection and heat dissipation of the package bottom plate.

Each capacitor is as close as possible to the CH275 related pins, at least two low ESR high-frequency capacitors between VHV and GND, fully connected to the PCB copper-laying GND, the PCB alignment with the chip GND pins is as short and thick as possible, and the capacitance withstand voltage should be higher than 150% of the supply voltage.

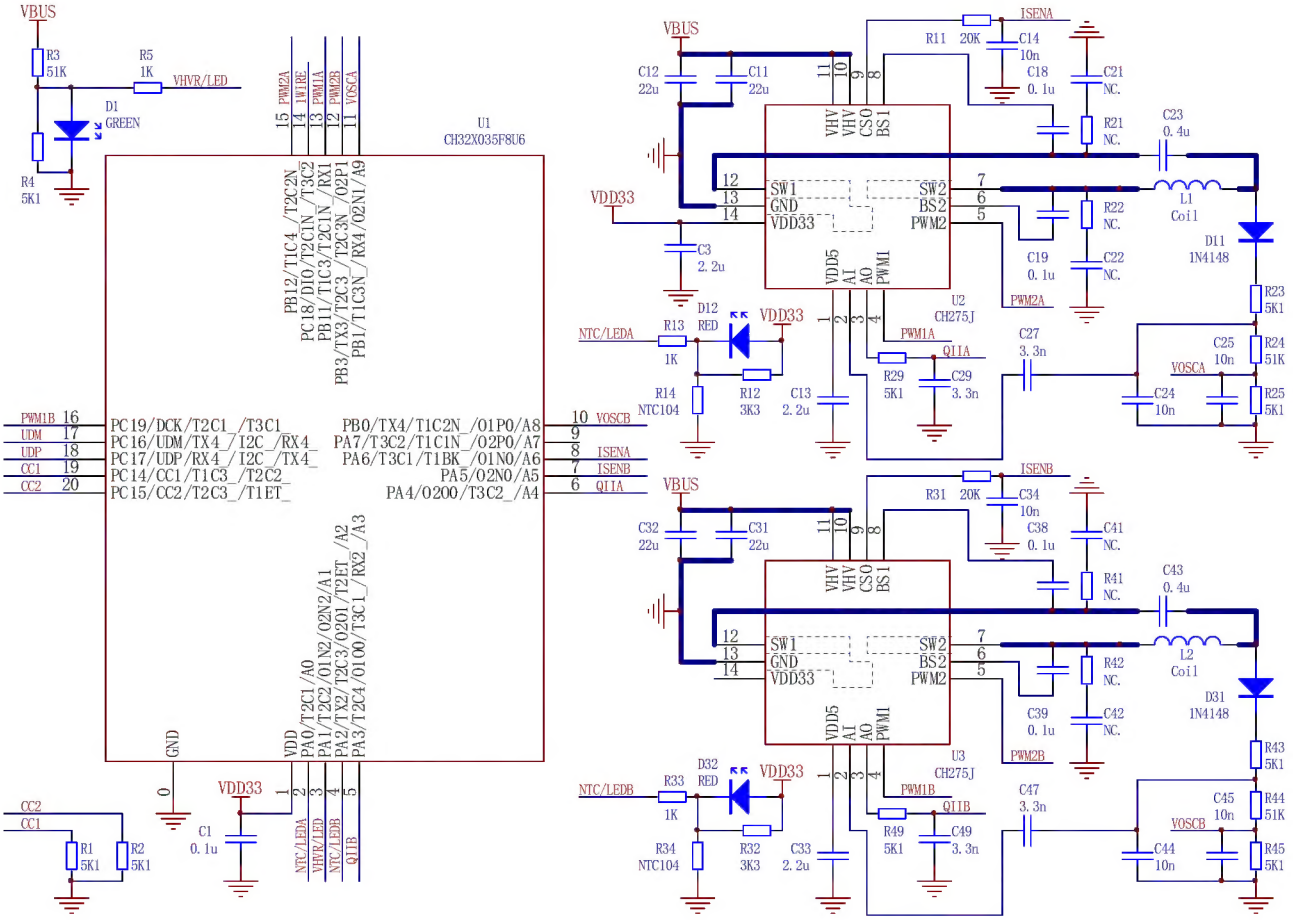
7.1 Dual-channel Wireless Charging

The RISC-V general MCU chip CH32X035 with built-in PD and USB and 2 groups of H-bridge driver chips CH275 are used to realize 2 independent wireless charging and power supply terminals. CH275 itself works at 5V, and MCU is powered by 3.3V generated by CH275, which is less noisy than 5V power supply. The signal between CH275 and MCU is at 3.3V level.

CH32X035F8U6 realizes PD high-power fast charging protocol through D+, D-, CC1 and CC2 pins, and supports Type-C and PDUSB; Sampling the working current of CH275 through ISEN pin; The voltage amplitude of the coil is sampled through the VOSC pin, which is convenient for foreign body detection; Input the feedback signal from the power receiving terminal through the QII pin and demodulate it. R29/C29 and R49/C49 are inserted between CH275 and MCU for RC low-pass filtering, or the input filtering function of PA3/PA4 of CH32X035 pin is enabled. The temperature is obtained by sampling the NTC voltage at the NTC/LED pin, and it is reused to drive the LED display by outputting a low level at the gap between the NTC/LED pins. The VHV voltage is sampled through the VHVR/LED pin, and it is reused to drive the LED display by outputting a high level at the gap between the VHVR/LED pins. If the LED is not needed, R5 can be short-circuited and D1 can be removed.

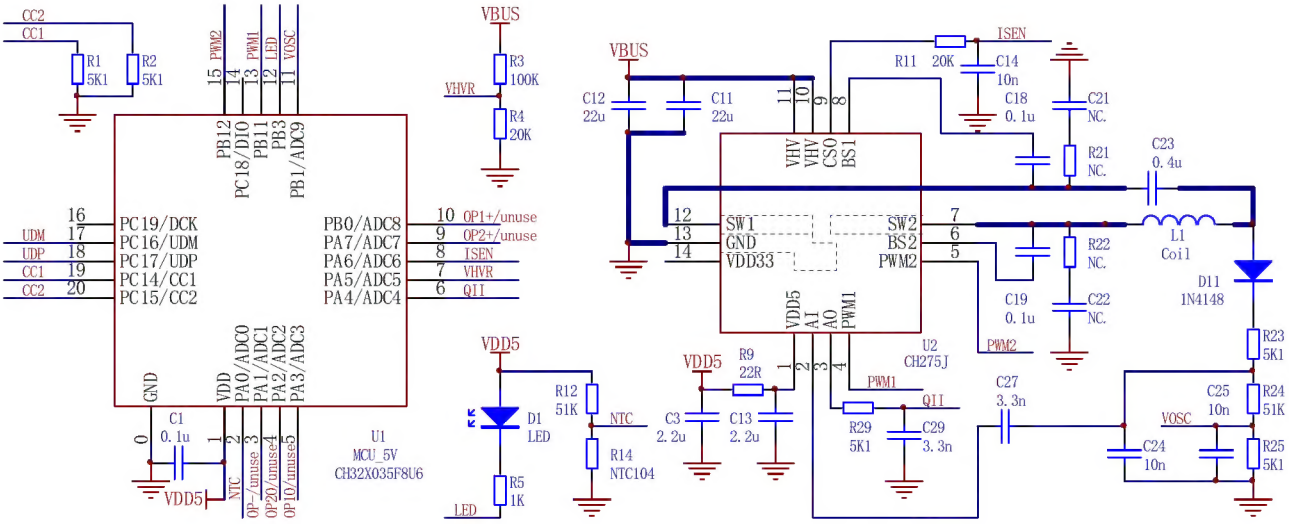
R29/C29, R49/C49 low-pass filter the signal and AC-couple it to the MCU pins via C28 and C48, and R18/R19, R38/R39 voltage divider to provide a DC bias (or implemented by the MCU's built-in pull-up or pull-down resistors) to adapt the input flip-flop voltages to the MCU pin levels.

PC18 pin of CH32X035 supports various 1-wire interfaces and is reserved for controlling multiple 1-wire RGB LED connected in series.


VBUS
R3 51K
R5 1K
VHVR/LED
D1 GREEN
R4 5K1
U1 CH32X035F8U6
PWM2A
1WIRE
PWM1A
PWM2B
VOSCA
PB12/T1C4_/T2C2N
PC18/DIO/T2C1N_/T3C2
PB11/T1C3/T2C1N_/RX1
PB3/TX3/T2C3_/T2C3N_/02P1
PB1/T1C3N_/RX4/02N1/A9
PWM1B 16
UDM 17
UDP 18
CC1 19
CC2 20
PC19/DCK/T2C1_/T3C1_
PC16/UDM/TX4_/I2C_/RX4_
PC17/UDP/RX4_/I2C_/TX4_
PC14/CC1/T1C3_/T2C2_
PC15/CC2/T2C3_/T1ET_
PB0/TX4/T1C2N_/01P0/A8
PA7/T3C2/T1C1N_/02P0/A7
PA6/T3C1/T1BK_/01N0/A6
PA5/02N0/A5
PA4/0200/T3C2_/A4
10 VOSCB
9
8 ISENA
7 ISENB
6 QI1A
GND
VDD
PA0/T2C1/A0
PA1/T2C2/01N2/02N2/A1
PA2/TX2/T2C3/0201/T2ET_/A2
PA3/T2C4/0100/T3C1_/RX2_/A3
0
VDD33
1
2
3
4
5
NTC/LEDA
VHVR/LED
NTC/LEDB
QI1B
CC2
CC1
R1 5K1
R2 5K1
C1 0.1u
VBUS
C12 22u
C11 22u
VHV
VHV
CS0
BS1
SW1
GND
VDD33
SW2
BS2
PWM2
C3 2.2u
VDD5
A1
A0
PWM1
U2 CH275J
D12 RED
R13 1K
R14 NTC104
R12 3K3
C13 2.2u
PWM1A
QI1A
R29 5K1
C29 3.3n
R11 20K
C14 10n
C18 0.1u
C21 NC.
R21 NC.
C23 0.4u
L1 Coil
C19 0.1u
C22 NC.
D11 1N4148
PWM2A
R23 5K1
C27 3.3n
C25 10n
R24 51K
VOSCA
C24 10n
R25 5K1
VBUS
C32 22u
C31 22u
U3 CH275J
D32 RED
R33 1K
R34 NTC104
R32 3K3
C33 2.2u
PWM1B
QI1B
R49 5K1
C49 3.3n
R31 20K
C34 10n
C38 0.1u
C41 NC.
R41 NC.
C43 0.4u
L2 Coil
C39 0.1u
C42 NC.
D31 1N4148
PWM2B
R43 5K1
C47 3.3n
C45 10n
R44 51K
VOSCB
C44 10n
R45 5K1

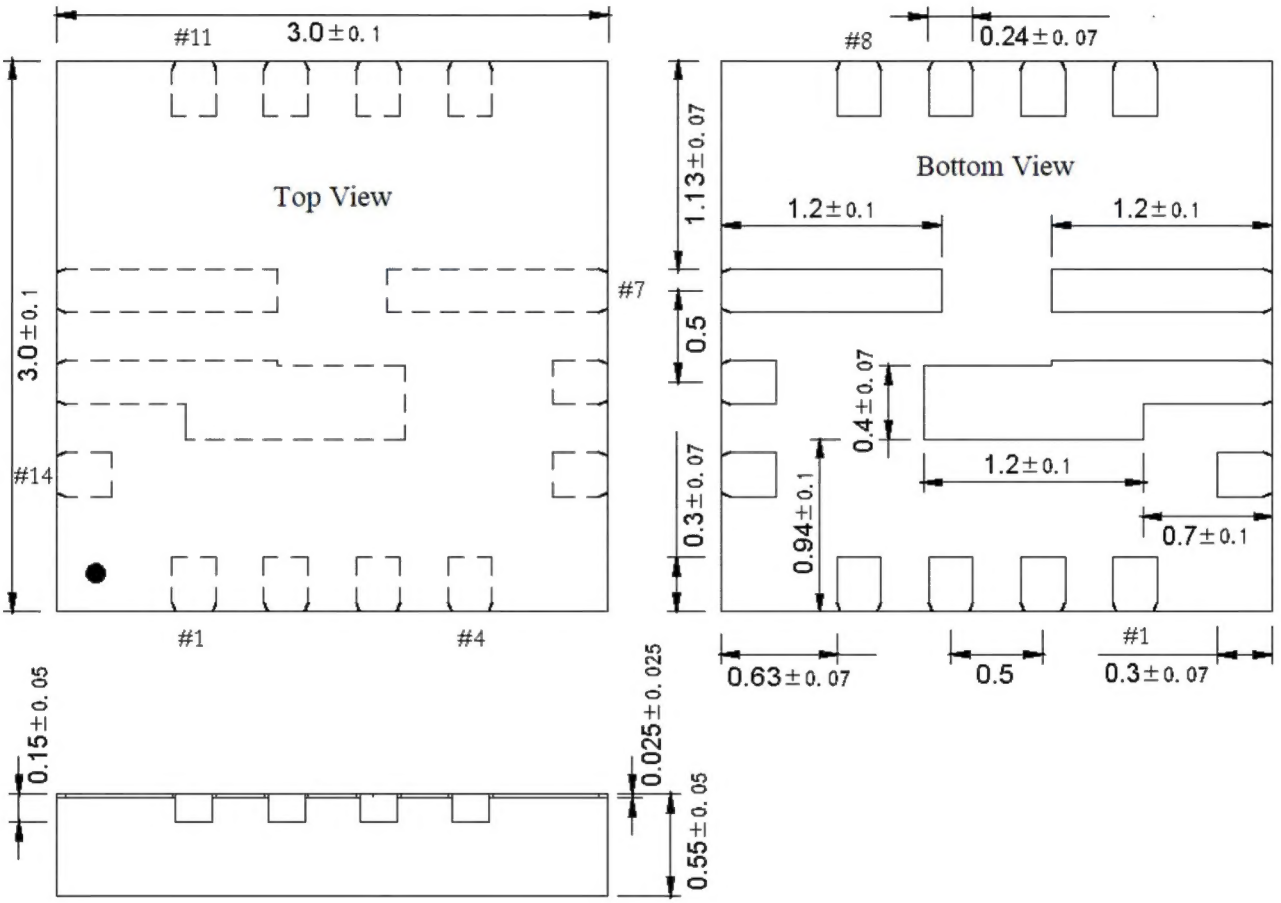
7.2 Connect the MCU with 5V Voltage.

The MCU is powered by CH275 from 20V to 5V, and the signal is 5V level. Optional R9 and C3 are used to simply filter the 5V power supply.



8. Package Information

The dimensions are in mm, and the differences are no more than ±0.1 for QFN packages.

8.1 QFN14F_3x3x0.55-0.5

The pins are all located at the Bottom. The length * width is 3*3, the thickness is 0.55, and the pin center-to-center spacing is 0.5.